FORZA

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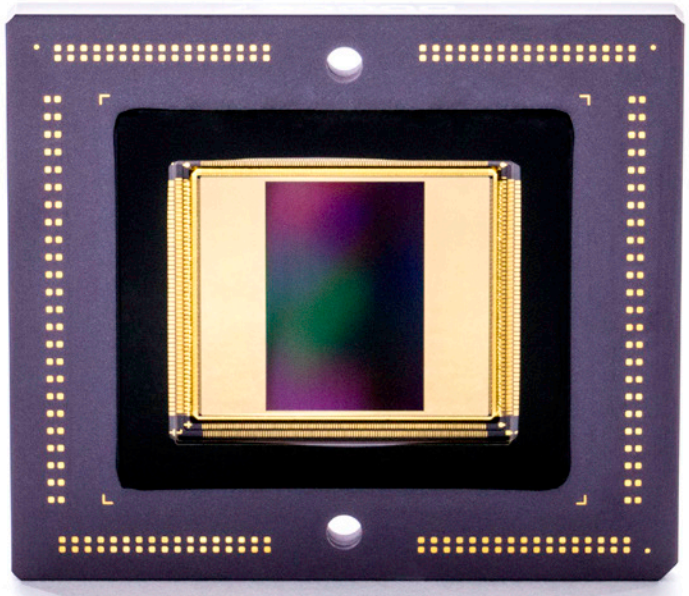


Optimizing BSI Sensor Yields With Integrated Production Services

An innovative manufacturing process enables the production of back side illumination sensors, driving improvements in high-speed imaging.

With speeds of over 1 million frames per second (fps), high-speed imaging is a critical research tool that can capture the most fleeting events in scientific and engineering applications. However, achieving these speeds comes with strings attached.

High frame rates are accompanied by small resolutions, which can make it challenging to see the subject matter. As frame rates increase, a pixel's exposure time to light decreases. These short exposure times require high levels of illumination to compensate for the short time the pixel receives light. For these reasons, many high-speed applications are light-starved; given the short exposure times at high frame rates, the available illumination can't deliver enough light to the camera's imaging sensor, producing a less-than-ideal or even unusable image.

To overcome these challenges, we recently partnered with Vision Research, a leading manufacturer of digital high-speed imaging systems, to design and manufacture a new kind of sensor that eases the speed-resolution-sensitivity constraint. This sensor employs back side illumination (BSI) to increase the pixel surface area that can capture photons.

Due to the size of high-speed image sensors and additional processing steps required, these sensors have traditionally been difficult to manufacture. "This is where our Integrated Production Services came in. Thanks to our expertise in prototype and wafer probe development, qualification and yield optimization, we were able to perfect the manufacturing process for the new BSI sensors and achieve practical yields," says Loc Duc Truong, Vice President of Engineering, Forza Silicon.

The result is the creation of a new kind of sensor that pushes the boundaries of speed in light-starved conditions.

LARGE SENSOR SIZE CREATES MANUFACTURING CHALLENGES

BSI sensors, which have been available for more than 10 years in smartphone and standard digital cameras, offer proven advantages when it comes to improving the low-light performance and dynamic range in consumer-focused cameras. So why did it take so long to bring these sensors to high-speed imaging? In a word, size.

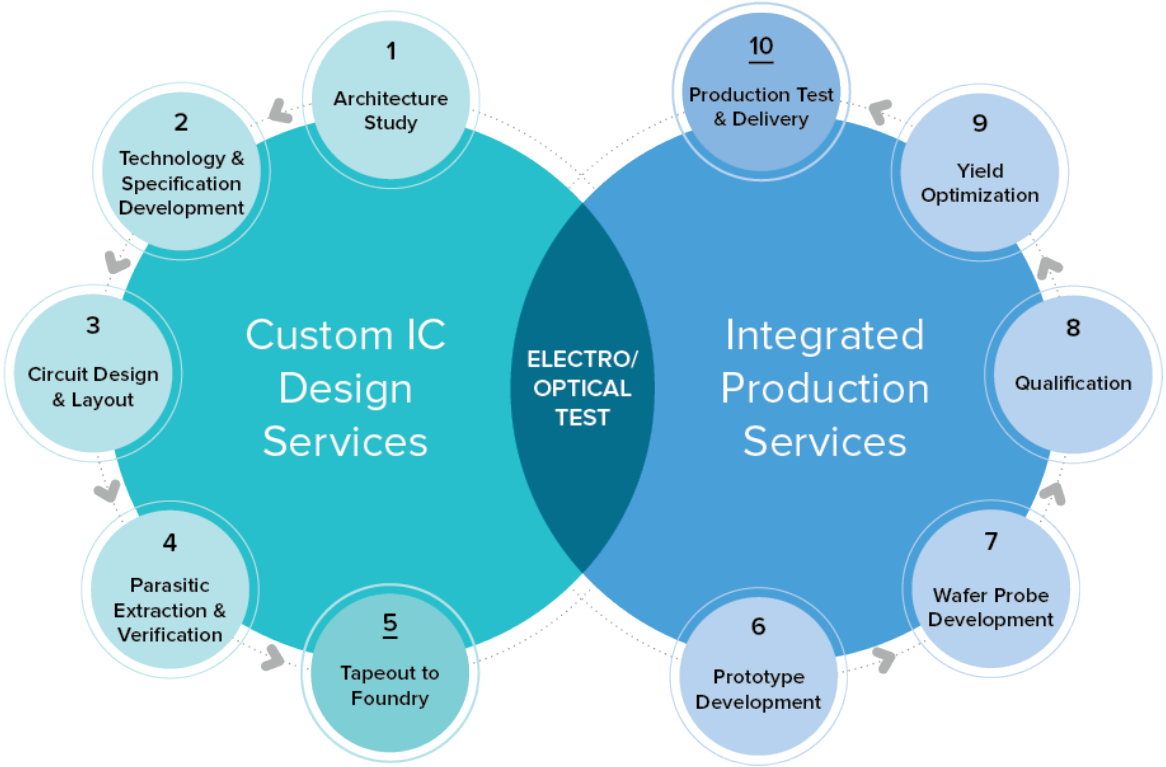
The sensors and pixels used in high-speed cameras are much larger than those in smartphone cameras and can't minimize the speed- resolution-sensitivity trade-offs. For instance, while a smartphone camera may have a pixel that measures less than 2 micrometers (µm) per side, many high-speed image sensor pixels are typically more than 6 µm and as much as 28 µm per side. As a direct result of the large pixel size, the die size is very large, creating a huge manufacturing challenge. For comparison, a typical smartphone sensor is approximately 7 x 6 millimeters (mm), while our sensor is 25 x 29 mm.

It is well-known that the semiconductor fabrication process is not 100 percent contamination-free. In an image sensor, a contaminating particle can take out a group of pixels or an entire row or column, rendering the sensor unusable. On a 300-mm wafer, approximately 1,400 smartphone sensors can be created versus approximately 70 high-speed sensors. Now, imagine having 100 "killer defects" randomly distributed on the wafer during the same fabrication process that makes a smartphone sensor and a high-speed sensor:

- In the smartphone sensor scenario, up to 100 dies would be lost, reducing the yield to a minimum of 92.9 percent (1,300/1,400).
- In the high-speed sensor scenario, we could lose anywhere between 40 to all 70 sensors depending on the distribution of defects, making the yield somewhere between 0 to 42.8 percent.

This number represents just the beginning of the yield loss, as additional losses can accumulate during the assembly process and final testing stage. The ability to manage and reduce these losses is therefore key to cost-effectively bringing large high-speed image sensors to market.

This is where our Integrated Production Services (IPS) shine. We work directly with the design teams during the design and layout of the sensor to minimize the effects of the "killer defects." We bring up and characterize the prototype sensors and work with our end-customers to integrate and optimize the sensor in the product camera. To this end, we have developed suites of optical and image processing methods to identify defects early in the wafer sort and assembly processes, enabling our IPS engineers to rapidly identify and address abnormal trends and also



An overview of our IPS capabilities.

provide insights into the nature of these issues. We also have excellent relationships and work closely with our fabrication, components, assembly and failure analysis partners to continuously monitor and improve yields. "Doing all of these activities — and more — allows us to achieve more practical sensor yields while reducing the time to market for our customers," Truong explains.

WHAT ARE FORZA INTEGRATED PRODUCTION SERVICES?

Our Integrated Production Services enable us to design and deliver custom analog mixed-signal integrated circuits (IC) and complementary metal oxide semiconductor (CMOS) imaging sensors. These in-house processes, which minimize risk, reduce cost and speed customers' time to market, consist of several steps:

- **Prototype development,** including package design and selection, as well as printed circuit board (PCB) and test system design services.
- **Wafer probe development** in our class 100 cleanroom, which is equipped with a 12-inch, fully automated wafer prober and optical fixture configuration. We also customize probe test programs and vectors with an optical stimulus.
- **Qualification services,** including electrostatic discharge (ESD), latch-up (LU), high-temperature operating life (HTOL), and shock and vibration tests. The ability to qualify designs to various JEDEC standards ensures high-quality, reliable products.
- **Yield optimization.** Our expertise lies in transitioning designs from the laboratory to the production floor to optimize customer yields. We also take advantage of our foundry relationships to improve design quality during the production process.
- **Production test and delivery.** Our team is experienced in turning prototype wafer probes, laboratory test programs and equipment into production-worthy sets of test protocols, leading to a product's final delivery.

Using these in-house production capabilities, we, along with Vision Research, overcome the manufacturing challenges associated with BSI sensor technology — and it has been well worth the wait.

UNLOCKING HIGH-SPEED BENEFITS

BSI sensor technology improves light sensitivity by placing the photoactive surface above the circuitry — a design that provides a direct route for photons and improves signal efficiency. Until now, the CMOS sensors used in high-speed cameras have been based on FSI architectures. In a traditional FSI architecture, the sensor's metal circuitry, which sits above the pixels' photodiodes, faces the light source. However, this metal circuitry prevents some incident light from reaching the pixels, which in turn affects the fill factor and reduces the sensor's sensitivity.

In order to address this issue, BSI sensors have a thick carrier wafer attached to the top of the metal stack. This arrangement allows the bulk silicon to be thinned and flipped, exposing the diodes that are facing the light source, as well as the metal surface behind them.

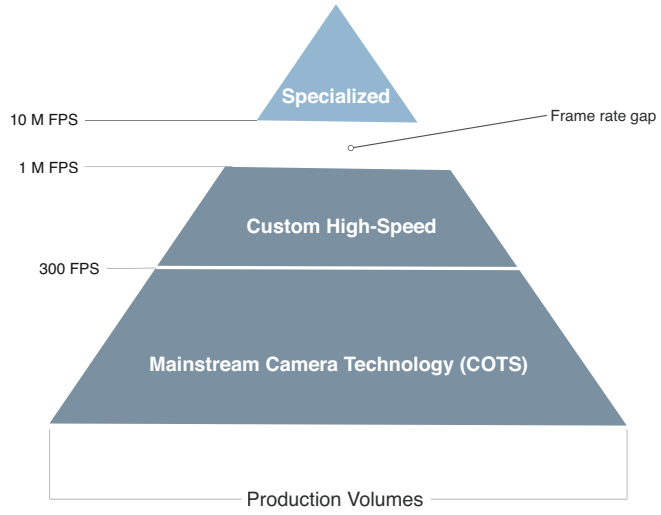
Thanks to these design features, BSI image sensors bring two significant advantages to high-speed applications: improved fill factor and improved processing speed:

SOLVING ANALOG-TO-DIGITAL CONVERSION CHALLENGES

Embedding analog-to-digital converters (ADC) on CMOS image sensors is standard practice, but the BSI sensor's speed required a massive increase in the amount of ADC. While modern CMOS image sensors typically have between 1,000 and 10,000 embedded ADC, the new BSI high-speed sensor has 40,000 ADC, each converting every 523 nanoseconds (ns) and generating a large amount of data to off-load from the sensor. To accomplish this task, the sensor incorporates 160 high-speed serial outputs operating at greater than 5 gigabytes per second (Gbps). This technology is common on central processing units (CPU) and Field Programmable Gate Arrays (FPGA) but new on a high-speed imaging sensor.

The density of ADC on the new sensor did create power management and electrical crosstalk challenges, which our engineers, together with Vision Research, solved. Since simulations are often used in predicting sensor performance, this sensor required the simulation to calculate for weeks to provide results. At Forza, we have significant experience in simplifying simulations and analyzing actual versus predicted results for fast design modifications.

In the case of the BSI sensor, testing of early designs revealed a higher level of ADC crosstalk in both normal imaging and binning modes than the simulation tools had predicted, causing noticeable artifacts in the images. Forza and Vision Research engineers discovered that the crosstalk exhibited predictable patterns and developed modeling techniques that eliminated the crosstalk altogether, which in turn mitigated imaging artifacts.



Back side illuminated (BSI) technology applied to high-speed imaging starts to close the frame rate performance gap between custom high-speed capability and specialized imaging capability.

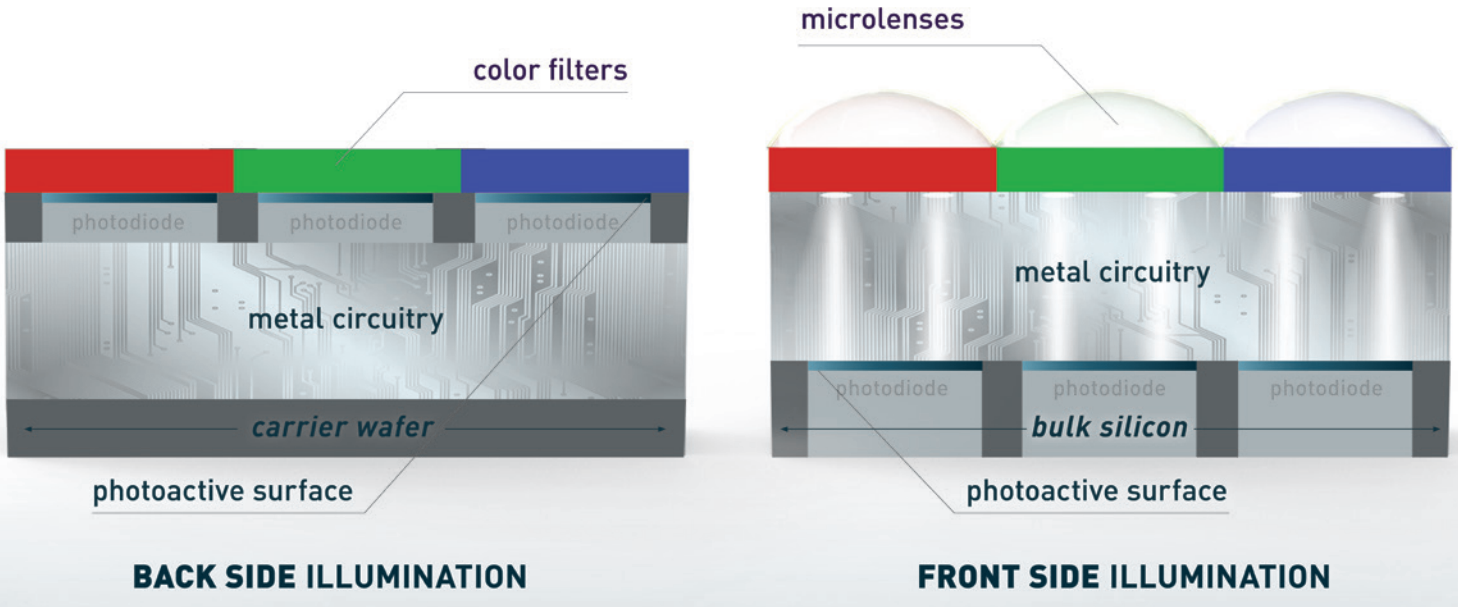
Providing a direct route for light improves fill factor. The effectiveness at capturing incident light is expressed in terms of the sensor's fill factor — or the percentage of the pixel surface area that can capture photons. Because the metal circuitry blocks or reflects some of the light, a typical FSI sensor will only have a fill factor between 50 and 60 percent.

On the other hand, by relocating the circuitry and providing a direct route for light to reach the light-receiving surface, BSI sensors achieve a fill factor close to 100 percent. These sensors also achieve a higher quantum efficiency (QE) throughout the visible light spectrum compared to FSI sensors. As an example of these improvements in action, the new BSI high-speed image sensor has a pixel size of 18.5 µm per side. Its proficiency at capturing light makes it about as sensitive at three times the speed as earlier FSI sensors with 28-µm pixels.

Adding more metal to the sensor's metal surface increases processing speed. The basic speed of the pixel array is limited by resistor-capacitor (RC) time constants. Adding metal reduces the resistance and increases the speed. In FSI sensors, however, the amount of metal on the sensor front is limited to allow light to reach the photodiodes — a constraint that leads to overhead in the processing speed. As frame rates increase and resolutions decrease, the camera can't provide maximum gigapixel/second (Gpx/sec) throughput because of these overhead losses.

Because BSI sensors don't have this constraint, they can have significantly increased metal circuitry, reducing or even eliminating the overhead. The metal can be moved to the back of the sensor, removing the need to create space to allow incident light to reach the pixels. Without this space requirement, the metal can be mapped more efficiently, thus removing the previous overhead in processing timing. This capability enables BSI sensors to maintain their maximum Gpx/sec throughput — even at very high frame rate/low resolution combinations.

CMOS Image Sensor Architectures



BSI sensors improve fill factor by providing a direct route for light to reach the light-receiving surface.

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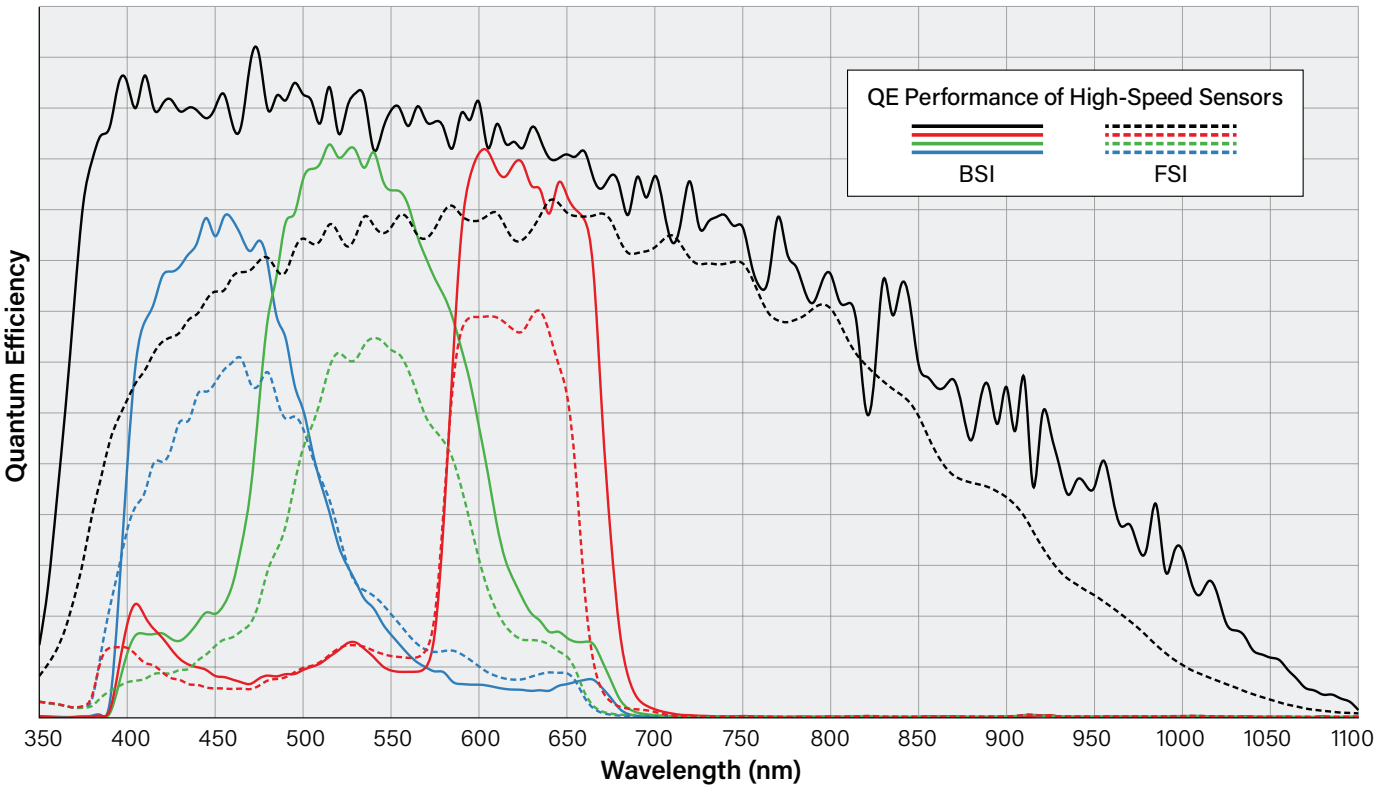
QE Comparison of BSI and FSI Sensors

Monochrome and Color



Compared with FSI sensors, BSI sensors achieve a higher quantum efficiency (QE) throughout the visible light spectrum.

BSI image sensors are also setting new standards for speed. The first high-speed camera to use this sensor technology — Vision Research's TMX 7510 — can capture images at 76,000 fps at full 1-megapixel (1280 x 800) resolution. It can also reach speeds more than an order of magnitude faster at reduced resolutions with binning. The camera tops out at 1.75 million fps with a resolution of 1280 x 32 and 640 x 64-pixel binned. Historically, the resolutions associated with frame rates above 1 million fps were too low for nearly all scientific uses, but 1280 x 32 represents a truly usable resolution in a wide range of testing applications.

Additional benefits of these cameras include exposure times as fast as 95 nanoseconds (ns) to truly freeze high-speed events, as well as the ability to partition the memory up to 511 times for rapid, repeat experiments in costly test settings.

THE BSI DIFFERENCE

BSI is not a new technology, and it has been used with great success in standard and smartphone cameras. By adapting the sensor design to high-speed imaging and using our IPS strategy to optimize manufacturing yields, we have been able to design and deliver a game-changing sensor that pushes the boundaries of high-speed imaging as we know it.

To learn more about our IPS capabilities and sensor technology, please visit: www.forzasilicon.com.

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